Ixp1200 Programming

An increasing number of system designers are using ASIP's rather than ASIC's to implement their system solutions. Building ASIPs: The Mescal Methodology gives a simple but comprehensive methodology for the design of these application-specific instruction processors (ASIPs). The key elements of this methodology are: Judiciously using benchmarking Inclusively identifying the architectural space Efficiently describing and evaluating the ASIPs Comprehensively exploring the design space Successfully deploying the ASIP This book includes demonstrations of applications of the methodologies using the Tipi research framework as

well as state-of-the-art commercial toolsets from CoWare and Tensilica. As the number of processor cores and IP blocks integrated on a single chip is steadily growing, a systematic approach to design the communication infrastructure becomes necessary. Different variants of packed switched on-chip networks have been proposed by several groups during the past two years. This book summarizes the state of the art of these efforts and discusses the major issues from the physical integration to architecture to operating systems and application interfaces. It also provides a guideline and vision about the direction this field is moving to. Moreover, the book outlines the consequences of adopting design platforms based on packet switched

network. The consequences may in fact be far reaching because many of the topics of distributed systems, distributed real-time systems, fault tolerant systems, parallel computer architecture, parallel programming as well as traditional system-on-chip issues will appear relevant but within the constraints of a single chip VLSI implementation.

This book constitutes the thoroughly refereed post proceedings of the International Conference on Information Networking, ICOIN 2004, held in Busan, Korea, in February 2004. The 104 revised full papers presented were carefully selected during two rounds of reviewing and revision. The papers are organized in topical sections on mobile Internet and

ubiquitous computing; QoS, measurement and performance analysis; high-speed network technologies; next generation Internet architecture; security; and Internet applications.

Advanced Web and Network Technologies, and Applications

Designing Embedded Communications Software

IFIP TC6 5th International Workshop, IWAN 2003, Kyoto, Japan, December 10-12, 2003, Revised Papers

IEEE Open Architectures and Network Programming Proceedings

Low-Power Processors and Systems on Chips

11th International Conference, Bangalore, India, December 19-22, 2004, Proceedings

Computer network devices need to be as easy for consumers to set up as stereo equipment. Universal Plug and Play (UPnP) is the technology that can make this happen. This book is primarily a software developer's guide for enabling UPnP, but it also provides a great introduction for those new to the technology.

Annotation - CD-ROM Includes the Intel Software Developers Kit and code for all programming examples.

This book constitutes the refereed proceedings of the 12th International Conference on Parallel Computing, Euro-Par 2006. The book presents 110 carefully reviewed, revised papers. Topics include support tools and environments; performance prediction and evaluation; scheduling and load balancing; compilers for high performance; parallel and distributed databases, data mining and

knowledge discovery; grid and cluster computing: models, middleware and architectures; parallel computer architecure and instruction-level parallelism; distributed systems and algorithms, and more.

Computer Technology and Computer Programming

The Journal of China Universities of Posts and Telecommunications

Programming Languages and Systems

Introduction to PCI Express

The Journal of the Computer Society of India

A Hardware and Software Developer's Guide

This book constitutes the refereed proceedings of the 7th International Workshop on Software and Compilers for Embedded

Systems, SCOPES 2003, held in Vienna, Austria in September 2003. The 26 revised full papers presented were carefully reviewed and selected from 43 submissions. The papers are organized in topical sections on code size reduction, code selection, loop optimizations, automatic retargeting, system design, register allocation, offset assignment, analysis and profiling, and memory and cache optimzations.
This book introduces the tools you'll need to program with the packetC

language. packetC speeds the development of applications that live within computer networks, the kind of programs that provide network functionality for connecting "clients" and "servers" and "clouds." The simplest examples provide packet switching and routing while more complex examples implement cyber security, broadband policies or cloud-based network infrastructure. Network applications, such as those processing digital voice and video, must be highly scalable,

secure and maintainable. Such application requirements translate to requirements for a network programming language that leverages massively-parallel systems and ensures a high level of security, while representing networking protocols and transactions in the simplest way possible. packetC meets these requirements with an intuitive approach to coarse-grained parallelism, with strong-typing and controlled memory access for security and with new data types

and operators that express the classic operations of the network-oriented world in familiar programming terms. No other language has addressed the full breadth of requirements for tractable parallelism, secure processing and usable constructs. The packetC language is growing in adoption and has been used to develop solutions operating in some of the world’s largest networks. This important new language, packetC, has now been successfully documented in this book, in which the

language's authors provide the materials and tools you'll need in a readable and accessible form.
This practical, how-to guide for programming the Intel IXP2400/2800 network processor family designed to help software and firmware engineers get up to speed quickly.
8th International Symposium, RAID 2005, Seattle, WA, USA, September 7-9, 2005, Revised Papers
A Software Developer's Guide to Universal Plug and Play
IXP1200 Programming

12th International Euro-Par Conference, Dresden, Germany, August 28-September 1, 2006, Proceedings

10th Asia-Pacific Conference, ACSAC 2005, Singapore, October 24-26, 2005, Proceedings

The Complete Microengine Coding Guide

This book constitutes the thoroughly refereed post-proceedings of the IFIP TC6 5th International Workshop on Active Networks, IWAN 2003, held in Kyoto, Japan, in December 2003. The 24 revised full papers presented were carefully reviewed and selected from 73 submissions. The papers are organized in

topical sections on high performance and network processors, high-level active network applications, low-level active network applications, self-organization of active services, experiences with service engineering for active networks, management in active networks, and selected topics in active networks.

本书主要介绍了网络处理器的概念和应用。先以Intel IXA 1200网络处理器的开发为例,介绍了网络处理器的特点、开发原理和开发方法;再以一个路由器的参考设计程序为例,介绍了网络处理器应用系统的开发。

The power consumption of microprocessors is one of the most important challenges of high-performance chips and portable devices. In chapters drawn from

Piguet's recently published Low-Power Electronics Design, this volume addresses the design of low-power microprocessors in deep submicron technologies. It provides a focused reference for specialists involved in systems-on-chips, from low-power microprocessors to DSP cores, reconfigurable processors, memories, ad-hoc networks, and embedded software. Low-Power Processors and Systems on Chips is organized into three broad sections for convenient access. The first section examines the design of digital signal processors for embedded applications and techniques for reducing dynamic and static power at the electrical and system levels. The second part describes several aspects of

low-power systems on chips, including hardware and embedded software aspects, efficient data storage, networks-on-chips, and applications such as routing strategies in wireless RF sensing and actuating devices. The final section discusses embedded software issues, including details on compilers, retargetable compilers, and coverification tools. Providing detailed examinations contributed by leading experts, Low-Power Processors and Systems on Chips supplies authoritative information on how to maintain high performance while lowering power consumption in modern processors and SoCs. It is a must-read for anyone designing modern computers or embedded systems.

International Conference on Compilers, Architecture, and Synthesis for Embedded Systems : October 30-November 1, 2003, San Jose, California, USA
APWeb 2006 International Workshops: XRA, IWSN, MEGA, and ICSE, Harbin, China, January 16-18, 2006, Proceedings
Building ASIPs: The Mescal Methodology
High Performance Embedded Architectures and Compilers
Proceedings, the Irish Signals and Systems Conference 2004
Programmable Networks for IP Service Deployment

Network System Design Using Network Processorsis the right book at the right time. Networking expert Douglas

Comer divides this book into four major sections: a quick review of basics and packet header formats; Traditional Protocol Processing Systems; Network Processors - an independent overview of the technology, including motivation, economics, inherent complexities, and various examples of commercial architectures; and Intel's network processor. Network processor complexity is boiled down and simplified by allowing readers to see example code for a commercial processor, detailed explanations on the motivation and economics behind the technology, and a glossary for

quick reference. The book's scope includes the concepts, principles, and hardware and software architectures that are the underpinnings of the design and implementation of network systems including routers, bridges, switches, intrusion detection systems, and firewalls - all independent of vendor specifics. An excellent fusion of network processing design principles, current architectures, and architectural directions, it is sure to become the standard text for this field the minute it hits the shelves.

This book constitutes the refereed proceedings of the 11th

International Conference on High-Performance Computing, HiPC 2004, held in Bangalore, India in December 2004. The 48 revised full papers presented were carefully reviewed and selected from 253 submissions. The papers are organized in topical sections on wireless network management, compilers and runtime systems, high performance scientific applications, peer-to-peer and storage systems, high performance processors and routers, grids and storage systems, energy-aware and high-performance networking, and distributed algorithms.

This book constitutes the refereed joint proceedings of four international workshops held in conjunction with the 8th Asia-Pacific Web Conference, APWeb 2006, in Harbin, China in January 2006. The 88 revised full papers and 58 revised short papers presented are very specific and contribute to enlarging the spectrum of the more general topics treated in the APWeb 2006 main conference.

UPnP Design by Example

ESOP ... : Proceedings

... International Workshop, RAID ... : Proceedings

Intel???????????

Using Network Processors : Intel IXP Version

CASES 2003

This book constitutes the refereed proceedings of the Second International Conference on High Performance Embedded Architectures and Compilers, HiPEAC 2007, held in Ghent, Belgium, in January 2007. The 19 revised full papers presented together with one invited keynote paper were carefully reviewed and selected from 65 submissions. The papers are organized in topical sections.

On behalf of the ProgramCommittee, we are pleased to present the

proceedings of the 2005 Asia-Paci?c Computer Systems Architecture Conference (ACSAC 2005) held in the beautiful and dynamic country of Singapore. This conference was the tenth in its series, one of the leading forums for sharing the emerging research ?ndings in this ?eld. In consultation with the ACSAC Steering Committee, we selected a - member Program Committee. This Program Committee represented a broad spectrum of research expertise to ensure a good balance of research areas, - stitutions and experience while maintaining the high quality of this conference

series. This year's committee was of the same size as last year but had 19 new faces. We received a total of 173 submissions which is 14% more than last year. Each paper was assigned to at least three and in some cases four ProgramC-mittee members for review. Wherever necessary, the committee members called upon the expertise of their colleagues to ensure the highest possible quality in the reviewing process. As a result, we received 415 reviews from the Program Committee members and their 105 co-reviewers whose names are acknowledged inthe proceedi

ngs.Theconferencecommitteead opteda systematicblind review process to provide a fair assessment of all submissions. In the end, we accepted 65 papers on a broad range of topics giving an acceptance rate of 37.5%. We are grateful to all the Program Committee members and the co-reviewers for their e?orts in completing the reviews within a tight schedule. This volume contains the 28 papers presented at ESOP 2004, the 13th European Symposium on Programming, which took place in Barcelona, Spain, March 29– 31, 2004. The ESOP series began in 1986 with the goal of

bridging the gap between theory and practice, and the conferences continue to be devoted to explaining fundamental issues in the speci?cation, analysis, and implementation of programming languages and systems. The volume begins with a summary of an invited contribution by Peter O'Hearn,titledResources, ConcurrencyandLocalReasoning ,andcontinueswith the 27 papers selected by the Program Committee from 118 submissions. Each submission was reviewed by at least three referees, and papers were selected during a ten-day

electronic discussion phase. I would like to sincerely thank the members of the Program Committee, as well as their subreferees, for their diligent work; Torben Amtoft, for helping me collect the papers for the proceedings; and Tiziana Margaria, Bernhard Ste?en, and their colleagues at MetaFrame, for the use of their conference management software.

The Microengine Coding Guide for the Intel IXP1200 Network Processor Family

A VLIW Approach to Architecture, Compilers and Tools

Issues and Practices

packetC Programming
Proceedings
Advances in Computer Systems Architecture
* Augment system performance * Optimize protocol implementation * Increase code maintainability Create network communications software with a thorough understanding of the essential system-level design and implementation choices and how they affect the p
The power consumption of integrated circuits is one of the most problematic considerations affecting the design of high-performance chips and portable devices. The study of power-saving design methodologies now must also include subjects such as systems on chips, embedded software, and the future of microelectronics. Low-Power

Electronics Design covers all major aspects of low-power design of ICs in deep submicron technologies and addresses emerging topics related to future design. This volume explores, in individual chapters written by expert authors, the many low-power techniques born during the past decade. It also discusses the many different domains and disciplines that impact power consumption, including processors, complex circuits, software, CAD tools, and energy sources and management. The authors delve into what many specialists predict about the future by presenting techniques that are promising but are not yet reality. They investigate nanotechnologies, optical circuits, ad hoc networks, e-textiles, as well as human powered sources of energy. Low-Power Electronics Design

delivers a complete picture of today's methods for reducing power, and also illustrates the advances in chip design that may be commonplace 10 or 15 years from now.

Today, programmable networks are being viewed as the solution for the fast, flexible and dynamic deployment of new telecommunications network services. At the vanguard of programmable network research is the Future Active IP Networks (FAIN) project. The authors of this book discuss their research in FAIN so you can get on the inside track to tomorrow's technology. Moreover, the book provides you with detailed guidelines for designing managed IP programmable networks.

Networks on Chip

7th International Workshop, SCOPES 2003, Vienna, Austria, September

24-26, 2003, Proceedings
Information Networking. Networking Technologies for Broadband and Mobile Networks
Recent Advances in Intrusion Detection
ISSC 2004, Queen's University Belfast, Northern Ireland, 30th June - 2nd July, 2004
13th European Symposium on Programming, ESOP 2004, Held as Part of the Joint European Conferences on Theory and Practice of Software, ETAPS 2004, Barcelona, Spain, March 29 - April 2, 2004, Proceedings
Network Processor Design: Issues and Practics, Volume 2 -- Contents -- Preface -- Chapter 1. Network Processors: Themes and Challenges, Patrick Crowley, Mark

Franklin, Haldun Hadimioglu, and Peter Z. Onufryk -- Part 1. Design Principles -- Chapter 2. A Programmable Scalable Platform for Next Generation Networking, Christos J. Georgiou, Valentina Salapura, and Monty Denneau -- Chapter 3. Power Considerations in Network Processor Design, Mark A. Franklin and Tilman Wolf -- Chapter 4. Worst-Case Execution Time Estimation for Hardware-assisted Multithreaded Processors, Patrick Crowley and Jean-Loup Baer -- Chapter 5. Multiprocessor Scheduling in Processor-based Router Platforms: Issues and Ideas, Anand Srinivasan, Philip Holman, James Anderson, Sanjoy Baruah and Jasleen Kaur -- Chapter 6. A

Massively Multithreaded Packet Processor, Steve Melvin, Mario Nemirovsky, Enric Musoll, Jeff Huynh, Rodolfo Milito, Hector Urdaneta, and Koroush Saraf -- Chapter 7. Exploring Trade-offs in Performance a ...

This book constitutes the refereed proceedings of the 8th International Symposium on Recent Advances in Intrusion Detection held in September 2005. The 15 revised full papers and two practical experience reports were carefully reviewed and selected from 83 submissions. The papers are organized in topical sections on worm detection and containment, anomaly detection, intrusion prevention and response, intrusion

detection based on system calls and network-based, as well as intrusion detection in mobile and wireless networks.

Over the past 12 years, ISSC has been a major forum for engineers and young researchers in Ireland on communications, control and DSP. The conference has established itself as one of the premier conferences in Ireland, addressing all aspects of signals and systems including design, implementation, algorithms, modelling and performance. This conference continued this tradition under the auspices of the IEE and for the first time the ISSC conference proceedings are published by the IEE and indexed

by INSPEC.

Next Generation Electronics

Active Networks

Software and Compilers for Embedded Systems

Programming Models for Application-specific Instruction Processors

Internet Telephone Monthly Newsletter

International Conference ICOIN 2004, Busan, Korea, February 18-20, 2004, Revised Selected Papers

Covering a broad range of new topics in computer technology and programming, this volume discusses encryption techniques, SQL generation, Web 2.0 technologies, and visual sensor networks. It also examines reconfigurable computing,

video streaming, animation techniques, and more. Readers will learn about an educational tool and game to help students learn computer programming. The book also explores a new medical technology paradigm centered on wireless technology and cloud computing designed to overcome the problems of increasing health technology costs.

This book highlights both the key achievements of electronic systems design targeting SoC implementation style, and the future challenges presented by the continuing scaling of CMOS technology.

Offering an overview, this guide details how 3GIO allows designers to overcome the practical performance limits of existing multidrop, parallel bus technology and explains how to increase performance and new

capabilities for a broad range of computing and communications platforms.

Network Processor Design

CASES ...

High Performance Computing - HiPC 2004

IXP2400/2800 Programming

Network Systems Design

Embedded Computing

The past few years have seen significant change in the landscape of high-end network processing. In response to the formidable challenges facing this emerging field, the editors of this series set out to survey the latest research and practices in the design, programming, and use of network processors. Through chapters on hardware, software, performance and modeling, Volume 3 illustrates the potential for new NP applications,

helping to lay a theoretical foundation for the architecture, evaluation, and programming of networking processors. Like Volume 2 of the series, Volume 3 further shifts the focus from achieving higher levels of packet processing performance to addressing other critical factors such as ease of programming, application developments, power, and performance prediction. In addition, Volume 3 emphasizes forward-looking, leading-edge research in the areas of architecture, tools and techniques, and applications such as high-speed intrusion detection and prevention system design, and the implementation of new interconnect standards. *Investigates current applications of network processor technology at Intel; Infineon Technologies; and NetModule.

Presents current research in network processor design in three distinct areas: *Architecture at Washington University, St. Louis; Oregon Health and Science University; University of Georgia; and North Carolina State University. *Tools and Techniques at University of Texas, Austin; Academy of Sciences, China; University of Paderborn, Germany; and University of Massachusetts, Amherst. *Applications at University of California, Berkeley; Universidad Complutense de Madrid, Spain; ETH Zurich, Switzerland; Georgia Institute of Technology; Vrije Universiteit, the Netherlands; and Universiteit Leiden, the Netherlands.

"Embedded Computing is enthralling in its clarity and exhilarating in its scope. If the technology you are working on is associated with VLIWs

or "embedded computing", then clearly it is imperative that you read this book. If you are involved in computer system design or programming, you must still read this book, because it will take you to places where the views are spectacular. You don't necessarily have to agree with every point the authors make, but you will understand what they are trying to say, and they will make you think." From the Foreword by Robert Colwell, R&E Colwell & Assoc. Inc The fact that there are more embedded computers than general-purpose computers and that we are impacted by hundreds of them every day is no longer news. What is news is that their increasing performance requirements, complexity and capabilities demand a new approach to their design. Fisher, Faraboschi, and Young describe a

new age of embedded computing design, in which the processor is central, making the approach radically distinct from contemporary practices of embedded systems design. They demonstrate why it is essential to take a computing-centric and system-design approach to the traditional elements of nonprogrammable components, peripherals, interconnects and buses. These elements must be unified in a system design with high-performance processor architectures, microarchitectures and compilers, and with the compilation tools, debuggers and simulators needed for application development. In this landmark text, the authors apply their expertise in highly interdisciplinary hardware/software development and VLIW processors to illustrate this change in embedded

computing. VLIW architectures have long been a popular choice in embedded systems design, and while VLIW is a running theme throughout the book, embedded computing is the core topic. Embedded Computing examines both in a book filled with fact and opinion based on the authors many years of R&D experience. Features: · Complemented by a unique, professional-quality embedded tool-chain on the authors' website, http://www.vliw.org/book · Combines technical depth with real-world experience · Comprehensively explains the differences between general purpose computing systems and embedded systems at the hardware, software, tools and operating system levels. · Uses concrete examples to explain and motivate the trade-offs.

System-on-Chip
Research and Strategies
Euro-Par 2006 Parallel Processing
Second International Conference, HiPEAC 2007, Ghent, Belgium, January 28-30, 2007. Proceedings
Low-Power Electronics Design